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# A Cost-Effective FPGA-based Fault Simulation Environment

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# Outline

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1. Motivation
2. FPGA-Based Fault Simulation Environment
3. ECC Case Study

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**Fault attacks** - Attackers inject faults to recover secrets.

- Glitches in power or clock supply.
- Optical attacks (e.g., laser).

**Powerful threat for cryptographic implementations**.

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**Cryptographic implementations must be protected.**

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  Voltage, light sensors.

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- Dedicated, algorithmic detection or prevention.
  E.g. point validity check for ECC.

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- General, algorithmic error detection methods.
  Duplication or redundancy.
- Dedicated, algorithmic detection or prevention.
  E.g. point validity check for ECC.

**Countermeasures must be verified**.

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**Laboratory.**

- Late in design flow.
- Highly complicated.
- Difficult to reach high coverage.

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- Difficult to reach high coverage.

**Simulation.**

- Earlier in design flow.
- Fault models for abstraction.
- High performance and coverage possible.

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Two choices for hardware simulation.

1. **Software-based simulation.**
   - Performance low for large designs.
2. **FPGA-based simulation.**
   - Performance high.

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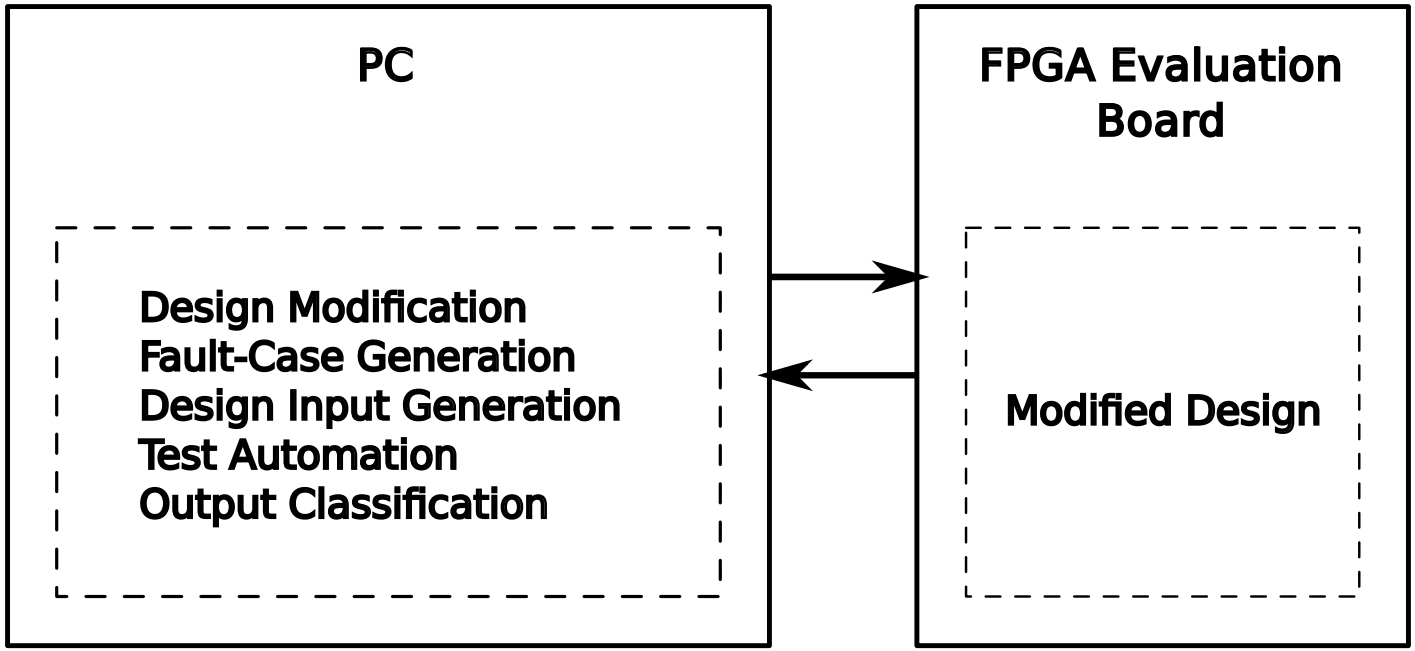
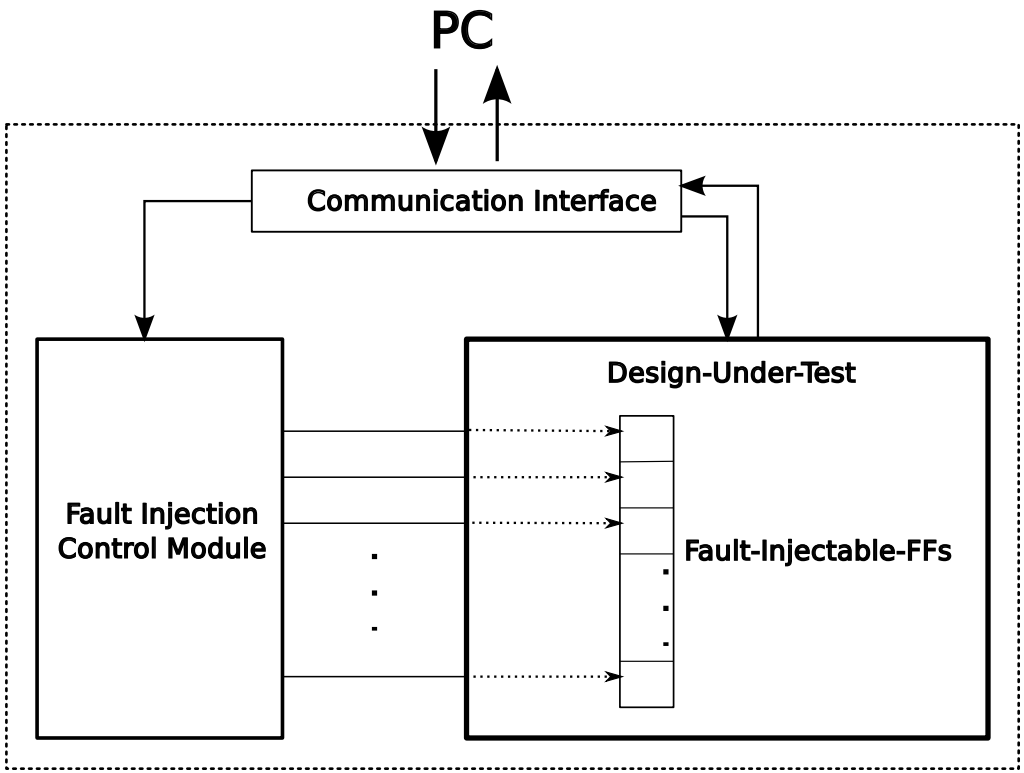
For digital hardware designs of cryptographic algorithms.



## Design-Under-Test (DUT) is modified through script.

- Replace flip-flops.
- Netlist.
- New top-level.
- Additional fault injection control and communication module.



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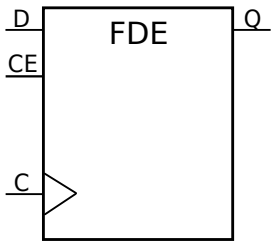
## Flip-flop cell replacement.



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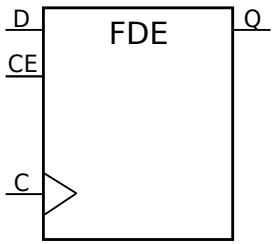
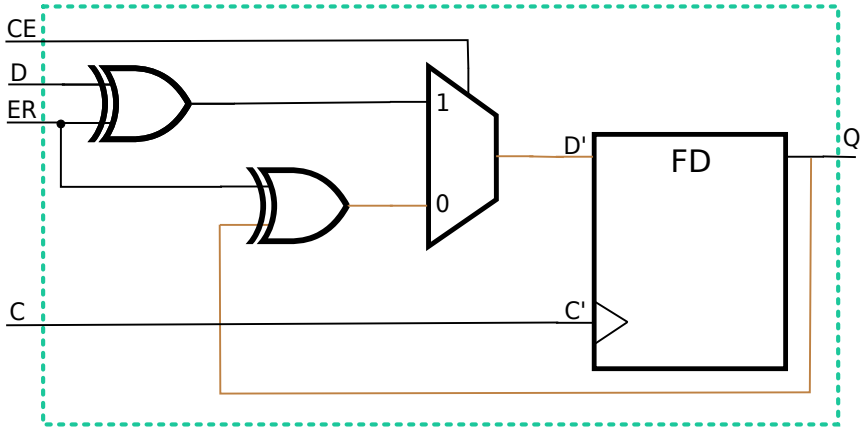
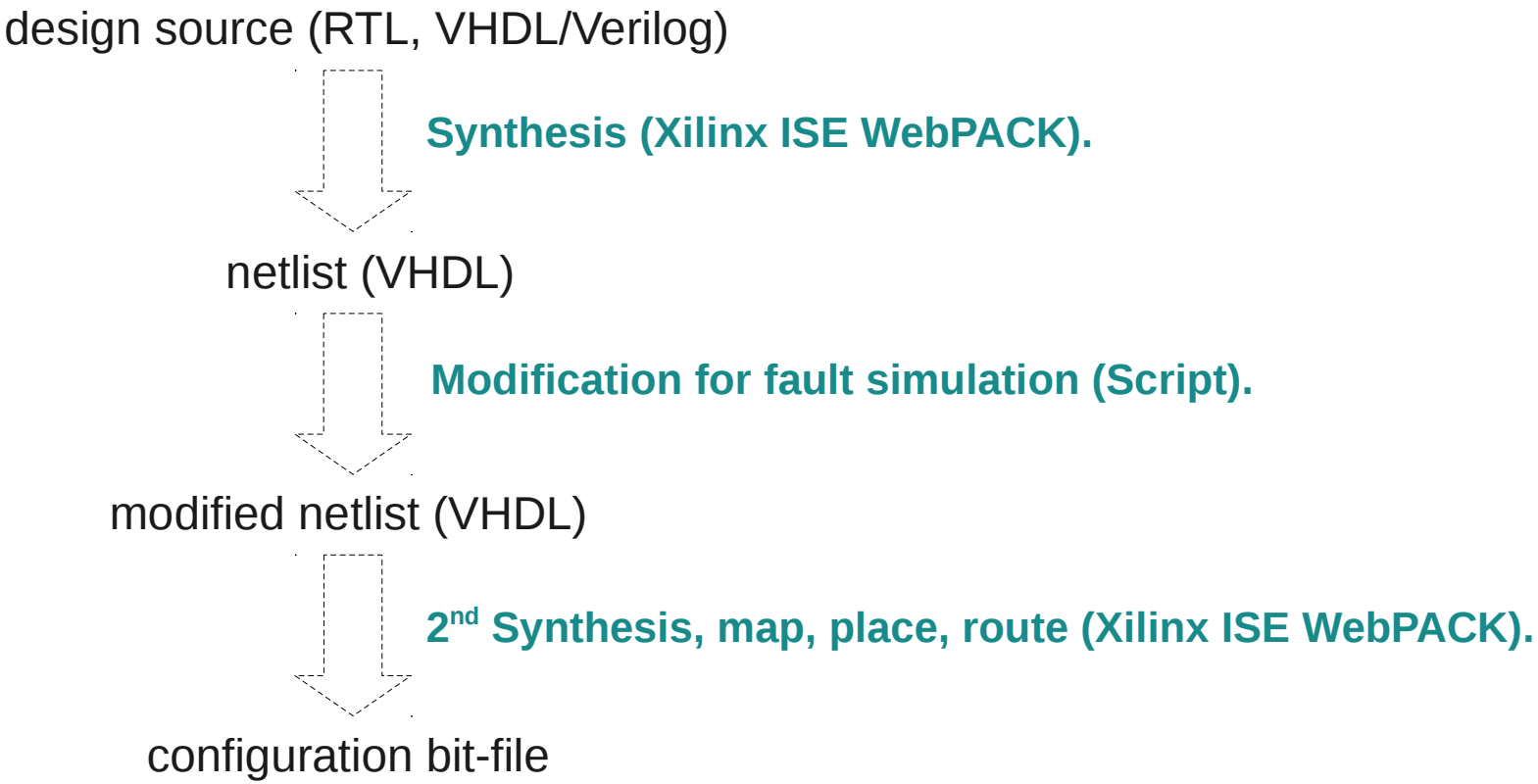
## Flip-flop cell replacement.



# Design Flow Integration

## FPGA-Based Fault Simulation Environment



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**Fault model specific for fault attacks**.

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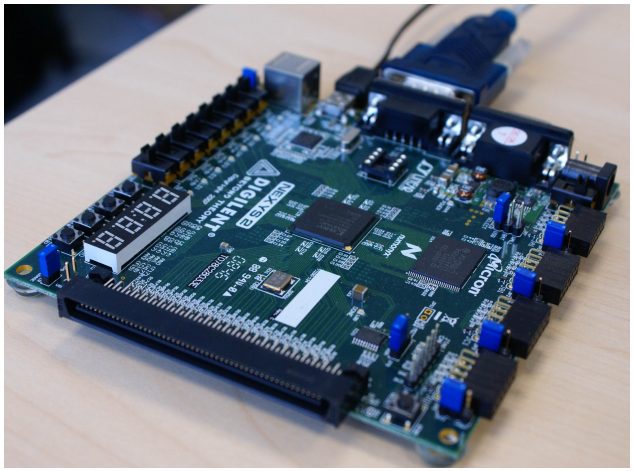
- Complete timing control.
- Complete location control.
  All single or multi-bit faults.
- Bit flip effect.
- Transient (one cycle) fault duration.

Fault model can be further restricted.

**Fault-case generation automated**.

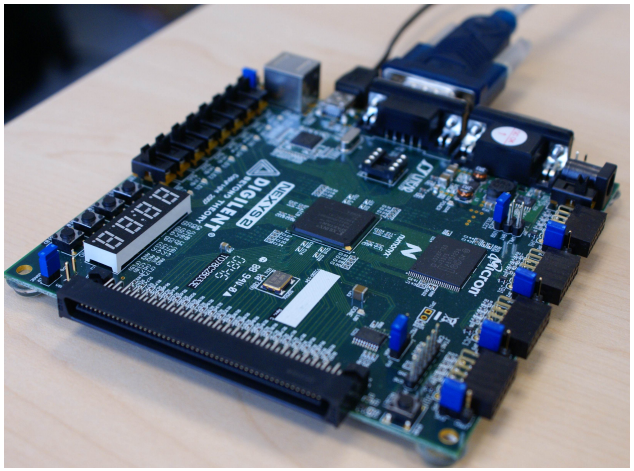
- Requires list of fault-injectable flip-flops.
- Requires fault configuration.
- Outputs list of fault test cases.
  If space to large, random choice of subset.

## **Simulation is automated**.



1. FPGA configured with modified design.
2. All fault cases are performed. For every case:

## **Simulation is automated**.



1. FPGA configured with modified design.
2. All fault cases are performed. For every case:
   - Fault injection control module re-configuration.
   - Start simulation.
   - Collect output and store testcase outcome.

**Available information.**

- DUT output vs. expected output.
- DUT status indication.
- Timing compliance.

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**Fault case simulation outcome.**

1. Silent - still correct.
2. Detected - detected fault.
3. Fault - faulty result output.
4. Timeout - No response.

# Simulation Environment Conclusion

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- **FPGA-based for high performance.**
- **Supports Verilog and VHDL designs.**
- **Automated modification on netlist - no design effort.**
- **Cost-effective Tooling.**

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**DUT** =
Digital hardware design of **Elliptic Curve Scalar Multiplication**.

- **Countermeasure** against fault attacks:
  **point validity check** at the end of computation.
  $\rightarrow$ This countermeasure is evaluated.

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**Fault model configuration:**

- Derived from fault attacks on ECC.
- Every clock cycle during ECSM.
  - $95,000$ cycles.
- Transient (one cycle) faults.
- Bit-flip fault effect.
- Single bit (to simplify case study) faults in all registers.
  Split simulation in two parts:
  - $1,600$ data-path flip-flops.
  - $90$ control-path flip-flops.

Fault injection **hardware overhead** for DUT $\sim +25\,\%$.

**Simulation performance** of 16 *ms* per test-case.

- DUT at **50** *MHz*.
- RS232 transmission more than **70%**.

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Simulation in two parts:

- **Control-path flip-flops.**
  - $\sim$ 9 million test-cases.
  - 100 % coverage.
- **Data-path flip-flops.**
  - $\sim$ 35 million test-cases.
  - 22 % coverage.

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9 **days of simulation** $\sim$ 46 years in software simulation.

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**Control-path**.

- 1 % Timeouts.
- 38 % Silent faults.
- 44 % Detected faults.
- 18 % **Faults**.
  In most cases program counter was manipulated and intermediate values output. → **Serious problem.** → **Countermeasure required**.

# Simulation Results, cont'd

ECC Case Study

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**Control-path**.

- 1 % Timeouts.
- 38 % Silent faults.
- 44 % Detected faults.
- 18 % **Faults**.
  In most cases program counter was manipulated and intermediate values output. → **Serious problem.** → **Countermeasure required**.

**Data-path**.

- 0 % Timeouts.
- 24 % Silent faults.
- 77 % Detected faults.
- 0.02 % **Faults**.
  Most changed output after point check. → **Useless for attacker**.

# Case Study Conclusion

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- **Speed-up of $\sim$ 2000 compared to software simulation.**
- **Point validity check countermeasure proved very effective.**
- **However, weaknesses were successfully exposed.**
  - **Control path needs protection.**
  - **Detected faults can be used for safe-error attacks.**