

Maël Gay



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AutoFault: Hardware-Oriented AFA Framework Multiple Fault Support

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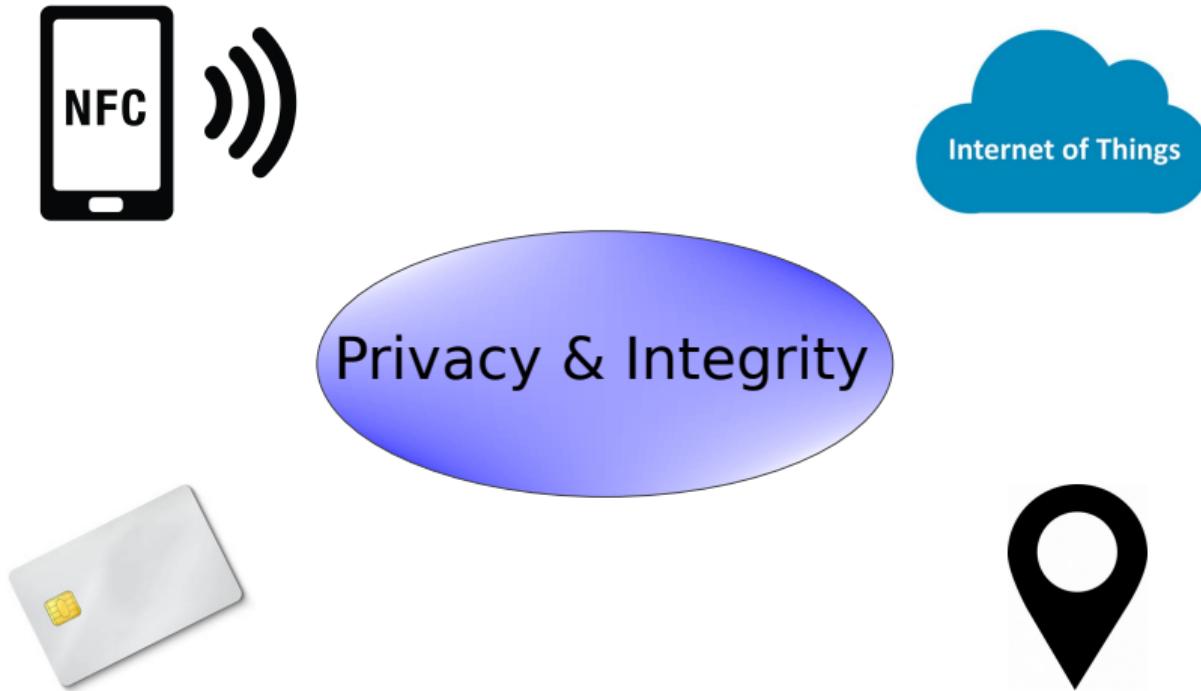
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Introduction

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Introduction

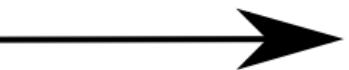


Cryptographic Primitives



- Cryptographic primitives

Cryptographic Primitives



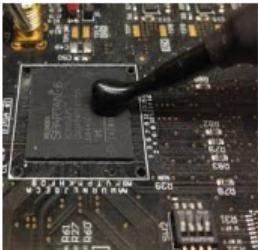
```
// -----
// Control signals
// -----
always @ (posedge clock or nesedge resetn) begin
    if ( resetn == 1'bz0 ) begin
        busy <= 1'bz0;
        start_flag <= 1'bz0;
        key_val <= 1'b0;
        round_n <= 4'b0;
    end
    else begin
        // Busy flag
        if ( !start || !busy ) busy <= 1'b1;
        else if ( !now_state == KEY_EXP ) 4k | round_n == n ) 4k | start_flag != 1'b1 ) busy <= 1'b0;
        else if ( ( now_state == ROUND_LOOP ) 4k | round_n == n ) busy <= 1'b0;
        else busy <= busy;
    end
    // Start flag
    if ( !start || start_flag == 1'b1 )
        start_flag <= 1'b0;
    else start_flag <= start_flag;
end
// Nr counter
if ( !next_state == IDLE ) round_n <= 4'b0;
else round_n <= round_n + 1'b1;
// Key valid flag
if ( ( now_state == KEY_EXP ) 4k | round_n == n ) key_val <= 1'b1;
else key_val <= key_val;
// Clock Selection
if ( ( now_state == ROUND_LOOP ) 4k | round_n == f_round ) 4k | fault_t == 1'b1 ) sel <= 1'b1;
else sel >= 1'b0;
end
```

- Hardware design -> physical restrictions

Cryptographic Primitives



```
// -----
// Control signals
// -----
always @(posedge clock orposedge resetn) begin
    if (! resetn == 1'b0) begin
        busy <= 1'b0;
        start_flag <= 1'b0;
        key_val <= 1'b0;
        round_n <= 4'b0;
        round_b <= 4'b0;
    end
    // Busy flag
    if (! start == 1'b1) | busy == 1'b1)
        busy <= 1'b1;
    else if ((now_state == "KEY_EXP") && (round_n == n)) |&| (start_flag == 1'b1) |&| busy == 1'b0)
        busy <= 1'b0;
    else busy <= busy;
    // Start flag
    if (! start == 1'b1) start_flag <= 1'b1;
    else if ((now_state == "ROUND_LOOP") && (round_n == n)) |&| (start_flag == 1'b0)
        start_flag <= start_flag;
    else start_flag <= start_flag;
    // Nr counter
    if (! next_state == "IDLE") round_n <= 4'b0;
    else round_n <= round_n + 1'b1;
    // Key valid flag
    if ((now_state == "KEY_EXP") && (round_n == n)) key_val <= 1'b1;
    else key_val <= key_val;
    // Clock Selection
    if ((now_state == "ROUND_LOOP") && (round_n == f_round) && (fault_t == 1'b1)) sel <= 1'b1;
    else sel <= 1'b0;
end
```

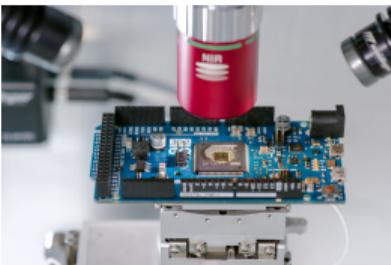
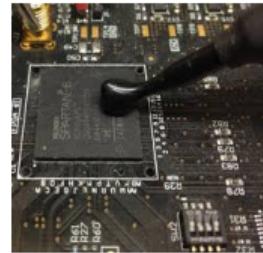


- Vulnerabilities, especially if physical access is allowed

Cryptographic Primitives

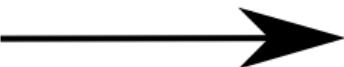


```
// Control signals  
// .....  
always @(posedge clock orposedge resetn) begin  
    if (resetn == 1'bo) begin  
        busy <= 1'bo;  
        start_flag <= 1'bo;  
        key_val <= 1'bo;  
        round_n <= 4'b00;  
    end  
    // Busy flag  
    if (start == 1'bl) | busy == 1'bl)  
        busy <= 1'bo;  
    else if ((new_state == "KEY_EXP") && (round_n == n)) | (start_flag == 1'bl) | busy == 1'bo)  
        busy <= busy;  
  
    // Start flag  
    if (start == 1'bl) start_flag <= 1'bo;  
    else if ((new_state == "ROUND_LOOP") && (round_n == n)) | start_flag == 1'bo)  
        start_flag <= start_flag;  
  
    // Nr counter  
    if (new_state == "IDLE") round_n <= 4'b00;  
    else round_n <= round_n + 1'bo;  
  
    // Key valid flag  
    if ((new_state == "KEY_EXP") && (round_n == n)) key_val <= 1'bo;  
    else key_val <= key_val;  
  
    // Clock Selection  
    if ((new_state == "ROUND_LOOP") && (round_n == f_round) && (fault_t == 1'bl)) sel <= 1'bl;  
    else sel >= 1'bo;  
end
```

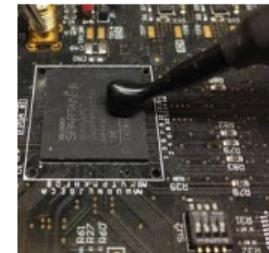


- Side-channel attacks: DPA, DFA...

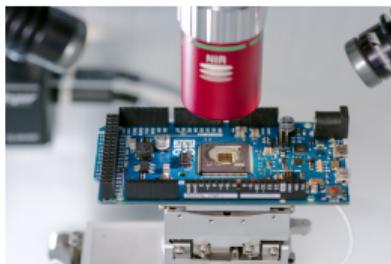
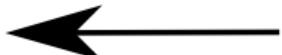
Cryptographic Primitives



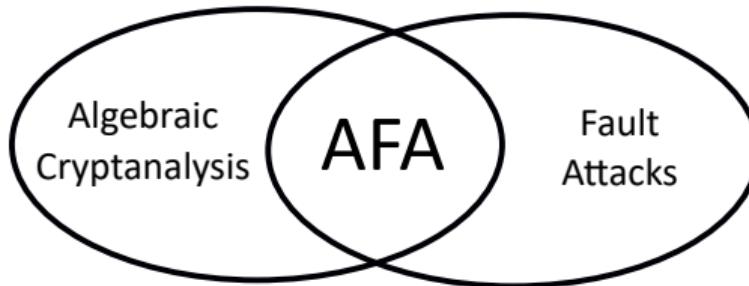
```
// -----
// Control signals
// -----
always @(posedge clock orposedge resetn) begin
    if (resetn == 1'b0) begin
        busy <= 1'b0;
        start_flag <= 1'b0;
        key_val <= 1'b0;
        round_n <= 4'b0;
        round_d <= 4'b0;
    end
    // Busy flag
    if (start == 1'b1) busy <= 1'b1;
    else if (new_state == "KEY_EXP") 4k | round_n == n) 4k | start_flag == 1'b1) busy <= 1'b0;
    else if ((new_state == "ROUND_LOOP") 4k | round_n == n) busy <= 1'b0;
    else busy <= busy;
    // Start flag
    if (start == 1'b1) start_flag <= 1'b1;
    else if (new_state == "ROUND_LOOP") start_flag <= 1'b0;
    else start_flag <= start_flag;
    // Nr rounds
    if (new_state == "IDLE") round_n <= 4'b0;
    else round_n <= round_n + 1'b1;
    // Key valid flag
    if ((new_state == "KEY_EXP") 4k | round_n == n)) key_val <= 1'b1;
    else key_val <= key_val;
    // Clock Selection
    if ((new_state == "ROUND_LOOP") 4k | round_n == f_round) 4k | fault_t == 1'b1)) sel <= 1'b1;
    else sel >= 1'b0;
end
```



- Focus: Algebraic Fault Attacks (AFA)



Algebraic Fault Attacks



- Input: description of the cipher, fault model & faulty values
- AFA frameworks:
 - Fault propagation and evaluation of the reduction of the key space
 - Solver that feeds functional description of the cipher and fault model to a SAT solver

AutoFault Framework Summary

- Objectives: automatic construction of fault attacks & evaluation of hardware implementations of cryptographic primitives
- Our framework focuses on:
 - Checking for vulnerabilities throughout each phase of the design
 - Evaluation of possible countermeasures
- Hardware description of the cipher as input
- Differences compared to previous frameworks:
 - Multiple fault injections
 - Different fault models
 - Support several SAT solvers
 - Speed-up of several orders of magnitude
- Easily repeatable for any changes in the hardware implementation
- May also be used to find new attacks

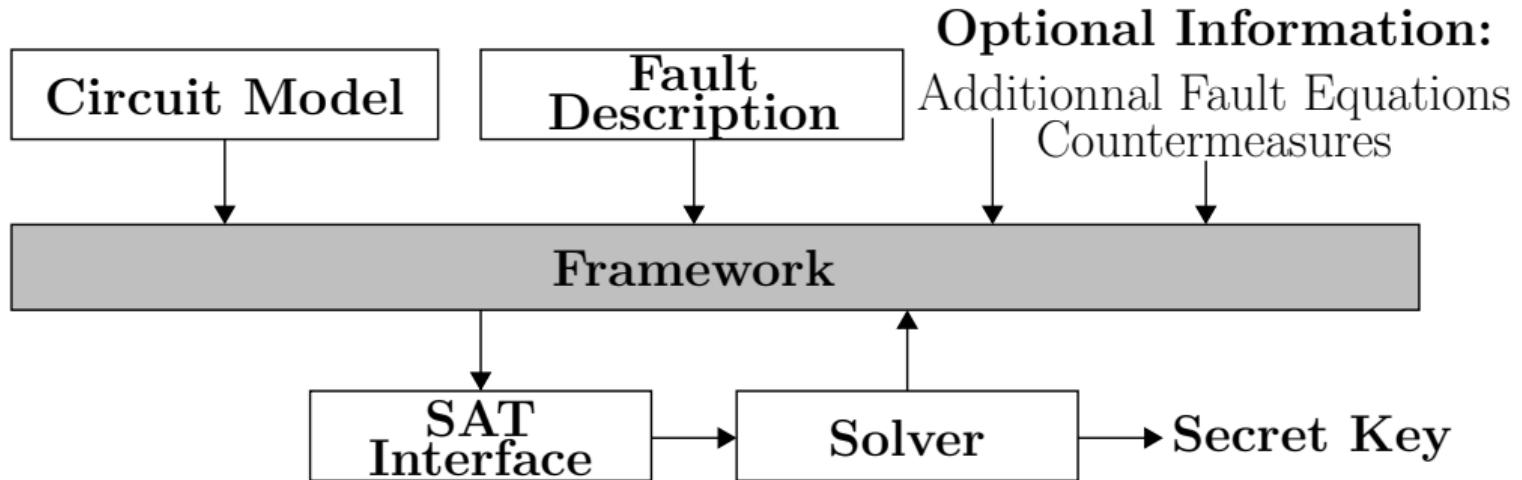
AutoFault Framework

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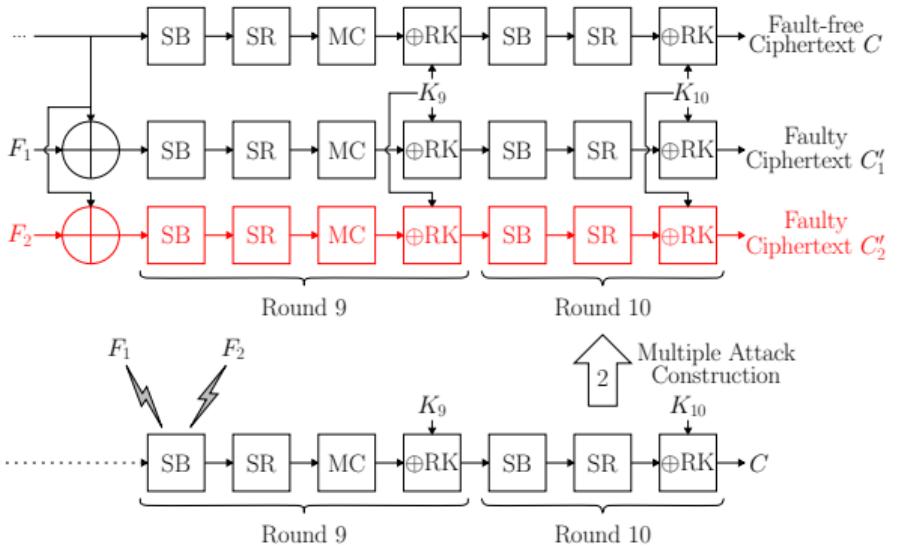
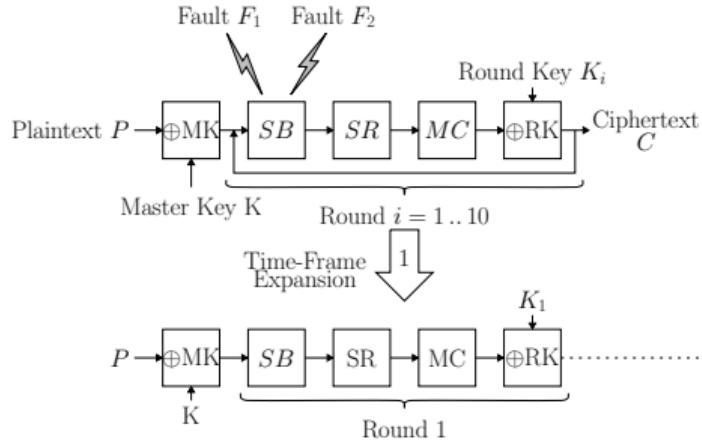
Framework Features

- Features:
 - Pre-silicon analysis
 - Post-silicon analysis
 - Validation of countermeasures
- Tools
 - Automated attack constructor **with multiple fault support**
 - Hardware to CNF converter
 - SAT solver interface
 - Attack simulation

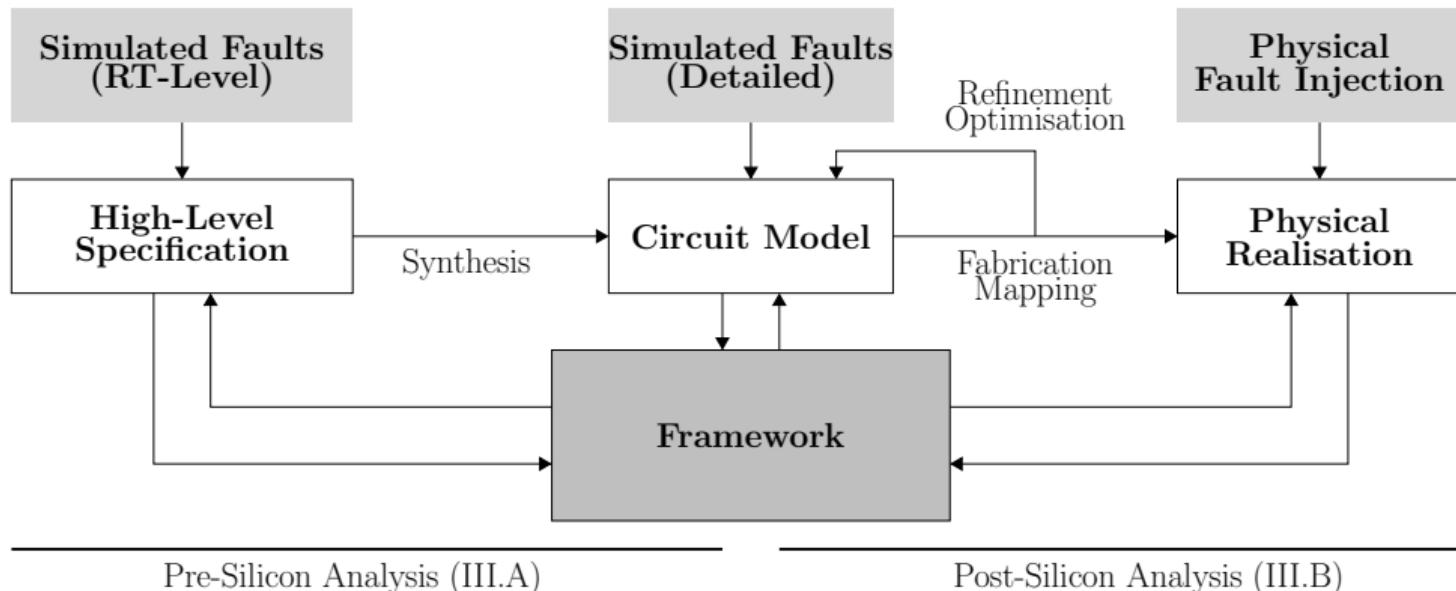
Overall Structure



Attack Construction



AutoFault during design flow

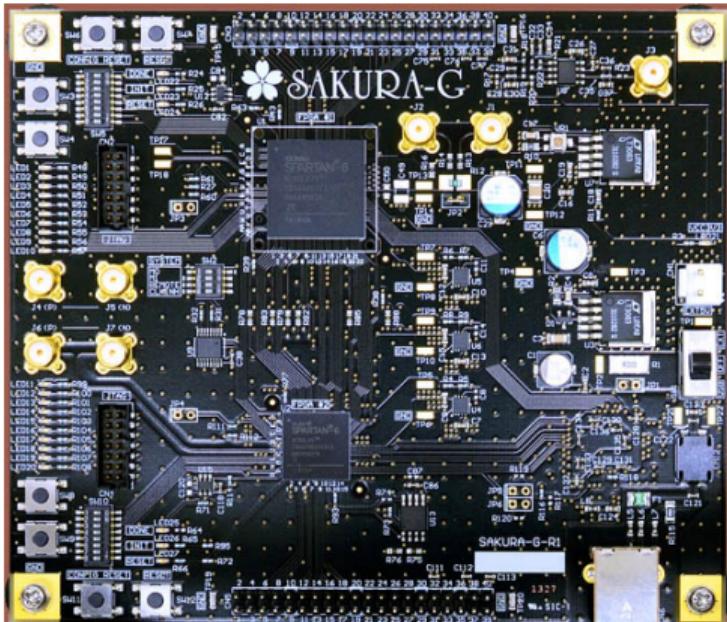


Experimental Results

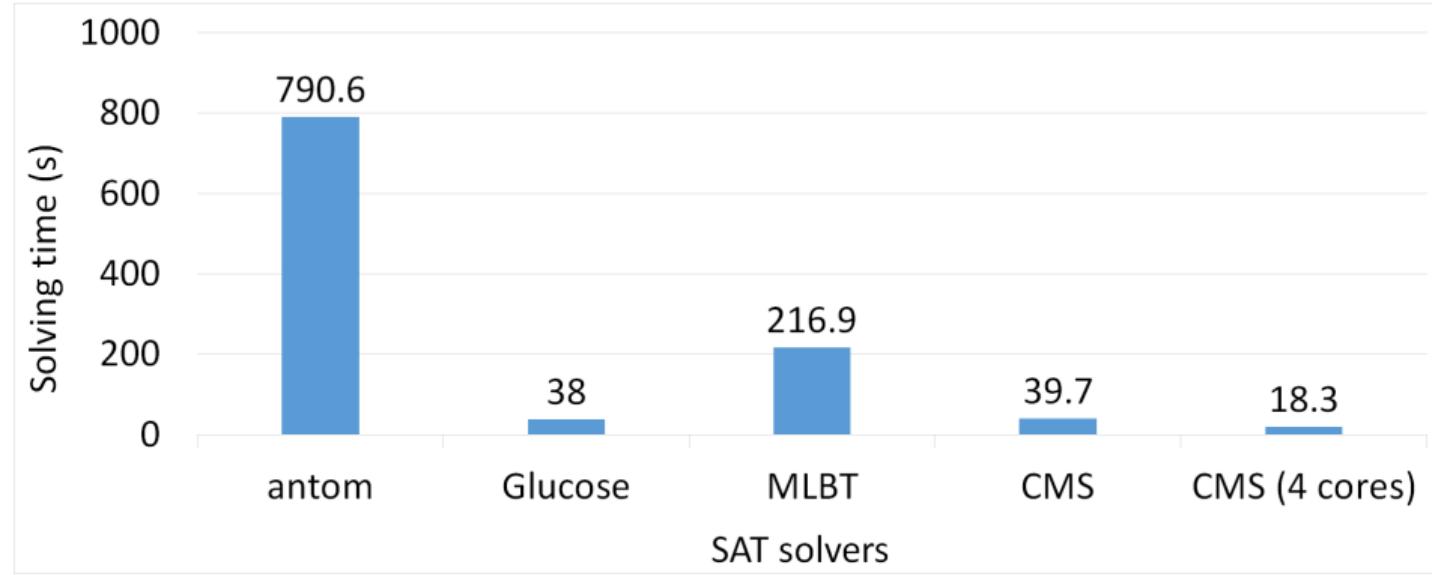
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Experimental Setup

- Intel Xeon processor with 4 cores at 3.3GHz
 - SAKURA-G FPGA board
 - Focus on Substitution and Permutation Network (SPN) ciphers



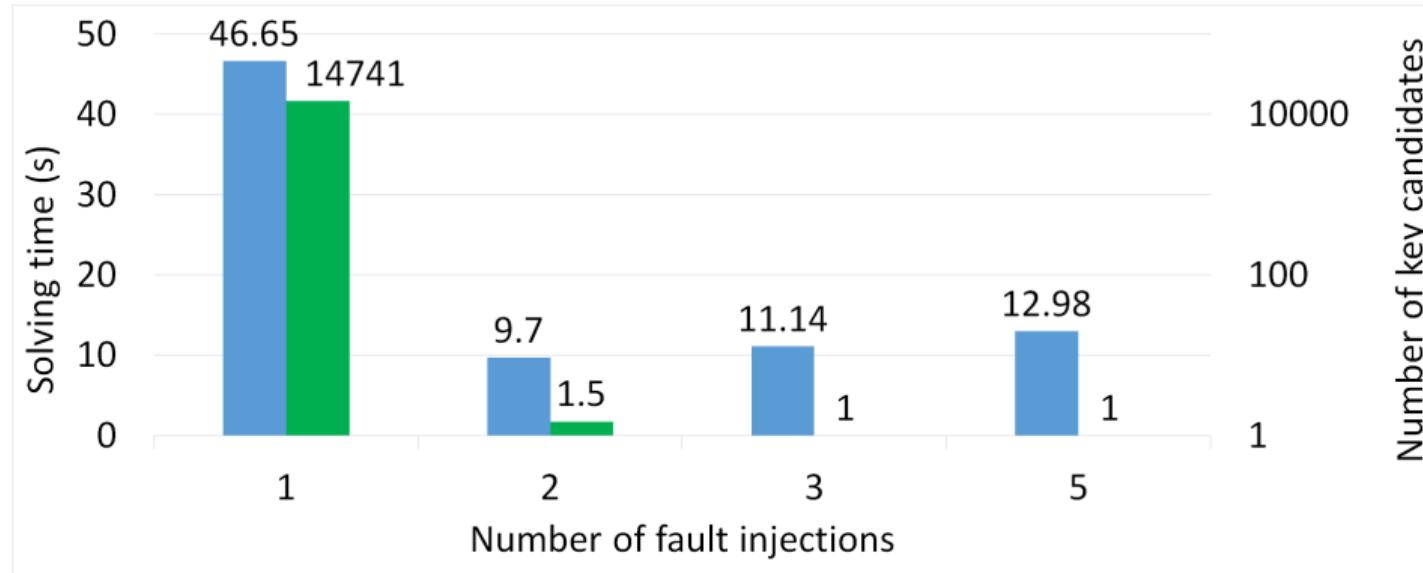
SAT Solver Comparison



Average solving times comparison between different SAT solver

- Small scale AES 444 & 2 fault injections
- MLBT: MapleLCMDistChronoBT & CMS: CryptoMiniSAT
- CMS was the best: in some instances, 2 orders of magnitude faster

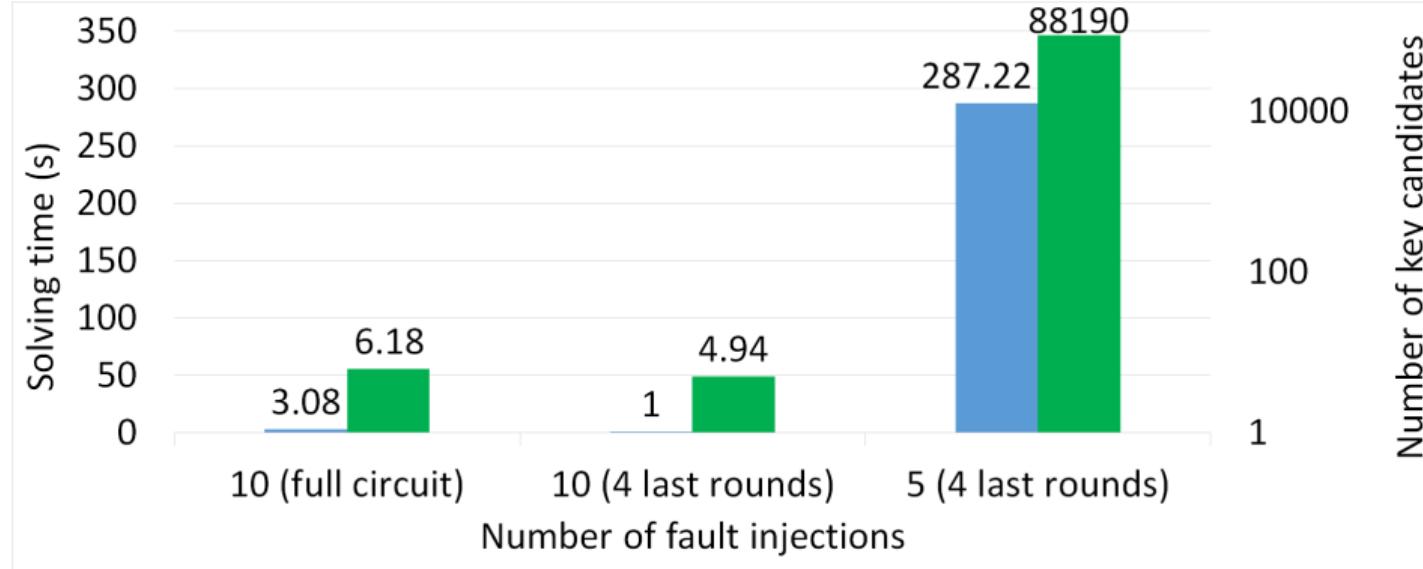
Multiple Fault Impact on LED Cipher



Average solving times and number of key candidates
LED64 using CMS (4 cores)

- Two fault injections is the most efficient, as more faults lead to larger solving times

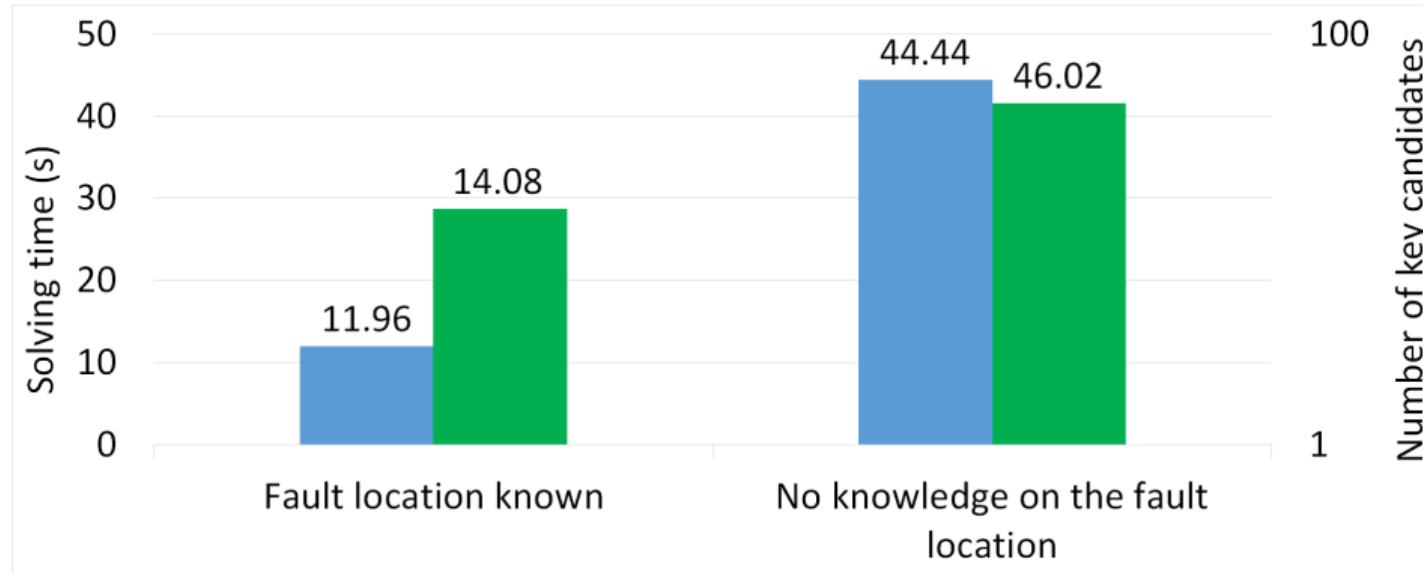
PRESENT Cipher



Average solving times and number of key candidates
PRESENT using CMS (4 cores)

- Successful attack with multiple faults
- More efficient to use only the relevant truncated circuit with multiple faults

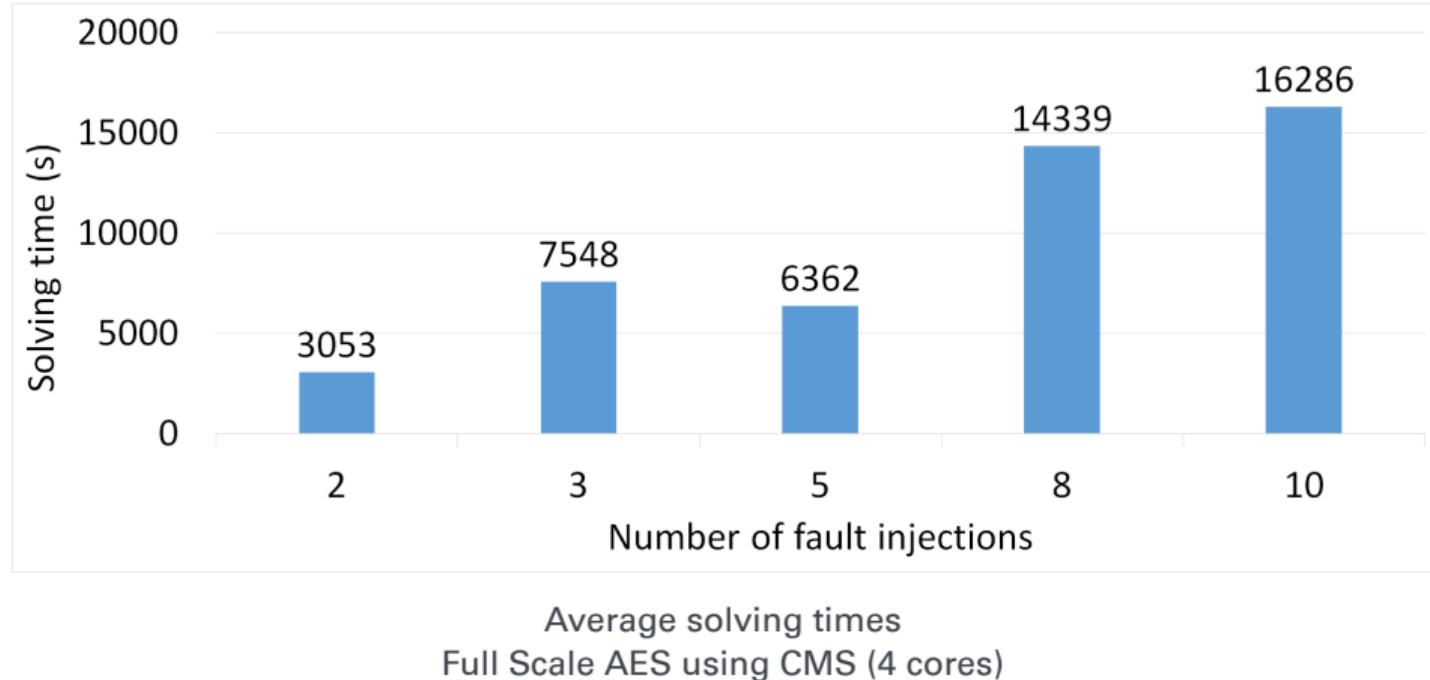
Unknown Nibble Attack Scenario on Small Scale AES



Average solving times and number of key candidates
Small Scale AES 224 using CMS (4 cores)

- AutoFault is able to solve without any fault location knowledge (longer runtime)

Application of AutoFault to a Full Scale AES



- With a single fault: 1 successful run (16 days)
- The support of multiple faults allows to solve for the full scale AES

Conclusion

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Comparison with Other AFA Frameworks

| AFA solver | Cipher description | Multiple faults support reported | Results for ciphers |
|------------------|--------------------|----------------------------------|---|
| XFC | Functional | no | AES, CLEFIA, SMS4 |
| Saha et al. | Functional | no | AES, PRESENT |
| Zhang et al. | Functional | yes | Piccolo, AES, DES, MIBS-64 LED, PRESENT, Twofish |
| Zhao et al. | Functional | no | LED |
| AutoFault (2017) | hardware-oriented | no | Small-scale AES, LED |
| AutoFault (2019) | hardware-oriented | yes | AES, LED, PRESENT |

Conclusion

- Evaluation of cryptographic implementation at multiple stages of the design
- Various fault model supported
- Support for multiple faults (attacks on AES & PRESENT)
- Successful attack on full scale AES
- Future work:
 - Impact of different countermeasures
 - Combine with side-channel analysis
 - Different solvers (algebraic)
 - Different class of cryptosystem (ECC, Post Quantum)



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